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10/660,053	09/11/2003	Hideaki Takizawa	1111.68332	7258

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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,053	TAKIZAWA ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *35-42 and 55-62* is/are allowed.

6)☒ Claim(s) *23-34 and 43-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/669,272.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/11/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The preliminary amendment filed on September 11th, 2003 has been entered.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 08/669,272, filed on May 29th, 1996.

Information Disclosure Statement

The Information Disclosure Statement filed on September 11th, 2003 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

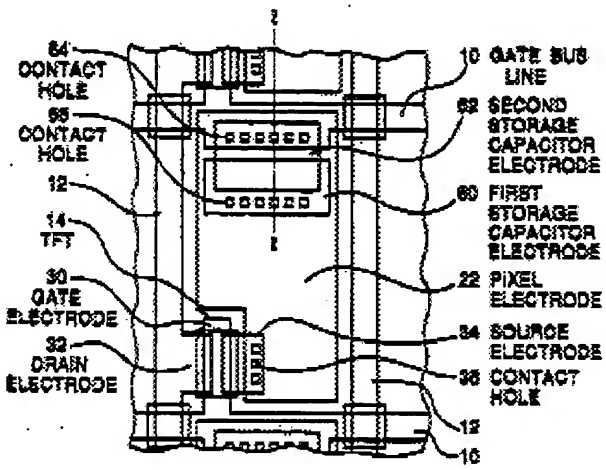
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 23-34 and 43-54 are rejected under 35 U.S.C. 102(b) as being anticipated by Ikeda et al. (U.S. Patent 5,182,661).

In re claim 23, **Ikeda** discloses a thin film transistor matrix device comprising: an insulating substrate; a plurality of thin film transistors **14** arranged on the insulating substrate **40** in a matrix; a plurality of picture element electrodes arranged on the insulating substrate in a matrix and connected to the thin film transistors; a plurality of bus lines **10** for commonly connecting the gates **30** of the thin film transistors **14**, the bus

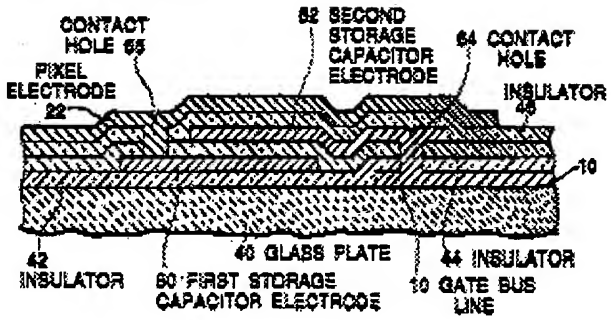
lines being made of a first conducting film (col. 4, lines 59 to col. 5, line 11 and FIGS. 3A-B);

FIGURE 3A



a first insulating film **44** formed on the first conducting film **60**; a second conducting film **62** formed on the first insulating film **44**; and a second insulating film **46** formed on the first insulating film **44** and the second conducting film **62**; wherein, outside an image display region, a first contact hole **64** is formed in the first insulating film **44** and the second insulating film through the first conducting film **60**, a second contact hole **66** is formed in the second insulating film **46** through the second conducting film **62** (col. 5, lines 12-40 and FIGS. 3A-B), and

FIGURE 3B



the first conducting film and the second conducting film electrically connect by a third conducting film **22** which is formed between the first contact hole and the second contact hole on the second insulating film (col. 5, line 4 to col. 6, line 21 and FIGS. 3A-6).

FIGURE 4A

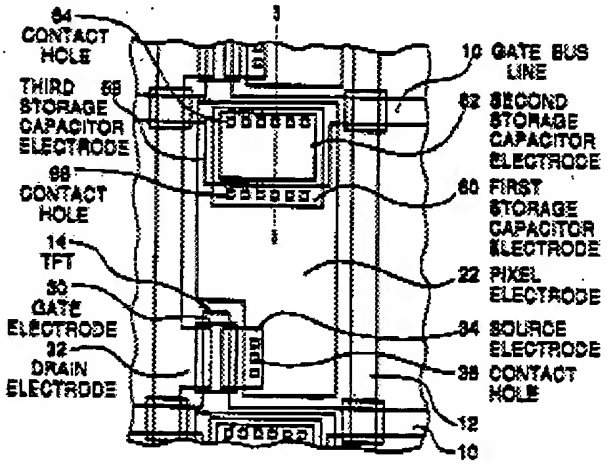
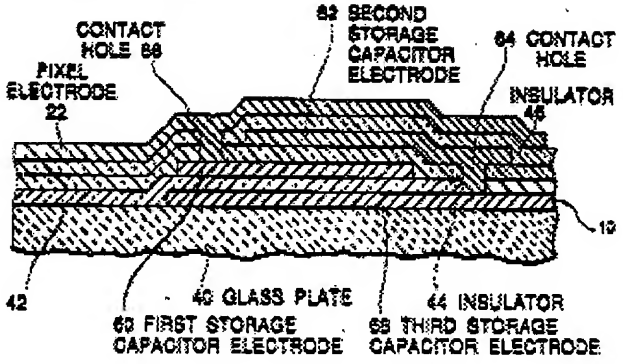


FIGURE 4B



In re claim 24, **Ikeda** discloses that a plurality of gate insulating films of the plurality of thin film transistors are made of the first insulating film (col. 5, lines 4-40 and FIGS. 3-6).

In re claim 25, **Ikeda** discloses that the third conducting film **22** is formed simultaneously with the plurality of picture element electrodes (col. 5, lines 4-40 and FIGS. 3-6).

In re claim 26, **Ikeda** discloses that the third conducting film **22** and the plurality of picture elements are made by Indium Tin Oxide (ITO) (col. 6, lines 4-11 and col. 6, line 14-21).

In re claim 27, **Ikeda** discloses that the first contact hole comprises a first hole of the first insulating film **44** and a second hole of the second insulating film **46**, and an axis of the first hole coincides with an axis of the second hole (FIGS. 3-6).

In re claim 28, **Ikeda** discloses that the first contact hole comprises a first hole of the first insulating film **44** and a second hole of the second insulating film **46**, and the first contact hole continues from the first hole to the second hole (FIGS. 3-6).

In re claim 29, **Ikeda** discloses a thin film transistor matrix device comprising: an insulating substrate; a plurality of thin film transistors **14** arranged on the insulating substrate **40** in a matrix; a plurality of picture element electrodes arranged on the insulating substrate in a matrix and connected to the thin film transistors; a plurality of bus lines **10** for commonly connecting the gates **30** of the thin film transistors **14**, the bus lines being made of a first conducting film (col. 4, lines 59 to col. 5, line 11 and FIGS. 3A-B); a first insulating film **44** formed on the first conducting film **60**; a first connection line for commonly crossing the plurality of bus lines, the first connection line being made of a second conducting film formed on the first insulating film; and a second conducting film **62** formed on the first insulating film **44**; and a second insulating film **46** formed on the first insulating film **44** and the second conducting film **62**, wherein, outside an image display region, a first contact hole **64** is formed in the first insulating film **44** and the second insulating film through the first conducting film **60**, a second contact hole **66** is formed in the second insulating film **46** through the second conducting film 62 (col. 5, lines 12-40 and FIGS. 3A-B), and each of the plurality of bus lines **10** is electrically connected to the first connection line through a third conducting film **22** which is formed between the first contact hole and the second contact hole on the second insulating film 46 (col. 5, line 4 to col. 6, line 21 and FIGS. 3A-6).

In re claim 30, **Ikeda** discloses that a plurality of gate insulating films of the plurality of thin film transistors are made of the first insulating film (col. 5, lines 4-40 and FIGS. 3-6).

In re claim 31, **Ikeda** discloses that the third conducting film **22** is formed simultaneously with the plurality of picture element electrodes (col. 5, lines 4-40 and FIGS. 3-6).

In re claim 32, **Ikeda** discloses that the third conducting film **22** and the plurality of picture elements are made by Indium Tin Oxide (ITO) (col. 6, lines 4-11 and col. 6, line 14-21).

In re claim 33, **Ikeda** discloses that the first contact hole comprises a first hole of the first insulating film **44** and a second hole of the second insulating film **46**, and an axis of the first hole coincides with an axis of the second hole (FIGS. 3-6).

In re claim 34, **Ikeda** discloses that the first contact hole comprises a first hole of the first insulating film **44** and a second hole of the second insulating film **46**, and the first contact hole continues from the first hole to the second hole (FIGS. 3-6).

In re claim 43, **Ikeda** discloses a thin film transistor matrix device comprising: an insulating substrate; a plurality of thin film transistors **14** arranged on the insulating substrate **40** in a matrix; a plurality of picture element electrodes arranged on the insulating substrate in a matrix and connected to the thin film transistors; a plurality of bus lines **10** for commonly connecting the gates **30** of the thin film transistors **14**, the bus lines being made of a first conducting film (col. 4, lines 59 to col. 5, line 11 and FIGS. 3A-B); a first insulating film **44** formed on the first conducting film **60**; a second conducting film **62** formed on the first insulating film **44**, the second conducting film comprising a non-doped Silicon film, a doped n^+-type Silicon film, and a metal film (col. 6, lines 36-52); and a second insulating film **46** formed on the first insulating film **44** and

the second conducting film **62**; wherein, outside an image display region, a first contact hole **64** is formed in the first insulating film **44** and the second insulating film through the first conducting film **60**, a second contact hole **66** is formed in the second insulating film **46** through the second conducting film **62** (col. 5, lines 12-40 and FIGS. 3A-B), and the first conducting film and the second conducting film electrically connect by a third conducting film **22** which is formed between the first contact hole and the second contact hole on the second insulating film (col. 5, line 4 to col. 6, line 21 and FIGS. 3A-6).

In re claim 44, **Ikeda** discloses that a plurality of gate insulating films of the plurality of thin film transistors are made of the first insulating film (col. 5, lines 4-40 and FIGS. 3-6).

In re claim 45, **Ikeda** discloses that the third conducting film **22** is formed simultaneously with the plurality of picture element electrodes (col. 5, lines 4-40 and FIGS. 3-6).

In re claim 46, **Ikeda** discloses that the third conducting film **22** and the plurality of picture elements are made by Indium Tin Oxide (ITO) (col. 6, lines 4-11 and col. 6, line 14-21).

In re claim 47, **Ikeda** discloses that the first contact hole comprises a first hole of the first insulating film **44** and a second hole of the second insulating film **46**, and an axis of the first hole coincides with an axis of the second hole (FIGS. 3-6).

In re claim 48, **Ikeda** discloses that the first contact hole comprises a first hole of the first insulating film **44** and a second hole of the second insulating film **46**, and the first contact hole continues from the first hole to the second hole (FIGS. 3-6).

In re claim 49, **Ikeda** discloses a thin film transistor matrix device comprising: an insulating substrate; a plurality of thin film transistors **14** arranged on the insulating substrate **40** in a matrix; a plurality of picture element electrodes arranged on the insulating substrate in a matrix and connected to the thin film transistors; a plurality of bus lines **10** for commonly connecting the gates **30** of the thin film transistors **14**, the bus lines being made of a first conducting film (col. 4, lines 59 to col. 5, line 11 and FIGS. 3A-B); a first insulating film **44** formed on the first conducting film **60**; a first connection line for commonly crossing the plurality of bus lines, the first connection line being made of a second conducting film **62** formed on the first insulating film, the second conducting film comprising a non-doped Silicon film, a doped n^+-type Silicon film, and a metal film (col. 6, lines 36-52); and a second insulating film **46** formed on the first insulating film **44** and the second conducting film **62**; wherein, outside an image display region, a first contact hole **64** is formed in the first insulating film **44** and the second insulating film through the first conducting film **60**, a second contact hole **66** is formed in the second insulating film **46** through the second conducting film **62** (col. 5, lines 12-40 and FIGS. 3A-B), and each of the plurality of bus lines **10** is electrically connected to the first connection line through a third conducting film **22** which is formed between the first contact hole and the second contact hole on the second insulating film **46** (col. 5, line 4 to col. 6, line 21 and FIGS. 3A-6).

In re claim 50, **Ikeda** discloses that a plurality of gate insulating films of the plurality of thin film transistors are made of the first insulating film (col. 5, lines 4-40 and FIGS. 3-6).

In re claim 51, **Ikeda** discloses that the third conducting film **22** is formed simultaneously with the plurality of picture element electrodes (col. 5, lines 4-40 and FIGS. 3-6).

In re claim 52, **Ikeda** discloses that the third conducting film **22** and the plurality of picture elements are made by Indium Tin Oxide (ITO) (col. 6, lines 4-11 and col. 6, line 14-21).

In re claim 53, **Ikeda** discloses that the first contact hole comprises a first hole of the first insulating film **44** and a second hole of the second insulating film **46**, and an axis of the first hole coincides with an axis of the second hole (FIGS. 3-6).

In re claim 54, **Ikeda** discloses that the first contact hole comprises a first hole of the first insulating film **44** and a second hole of the second insulating film **46**, and the first contact hole continues from the first hole to the second hole (FIGS. 3-6).

Allowable Subject Matter

Claims 35-42 and 55-62 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
December 20th, 2004

W. DAVID COLEMAN
PRIMARY EXAMINER